

In re Patent Application of:  
**RAYNOR, ET AL.**  
Serial No. 09/993,387  
Confirmation No. 4936  
Filing Date: November 16, 2001

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In the Claims:

Claims 1 to 10 (Cancelled).

11. (Currently Amended) A solid state imaging device comprising:

a two-dimensional array of pixels defining an image plane, the image plane comprising more than three rows of pixels;

readout electronics comprising a plurality of store circuits laterally adjacent the image plane for reading signals therefrom, with a store circuit corresponding to each pixel and comprising

a first store circuitry ~~circuit~~ for storing a reset value, and

a second store circuitry ~~circuit~~ for storing a read out value, with the read out value of a given pixel being modified by the stored reset value for that pixel; and

a multiconductor signal bus connected between said array of pixels and said readout electronics, said multiconductor bus comprising a respective conductor to provide a dedicated readout channel for only one pixel of said two-dimensional array of pixels defining the image plane.

Claim 12 (Cancelled).

13. (Previously Presented) A solid state imaging device according to Claim 11, wherein each pixel comprises:

a photosensitive diode; and

a switching circuit for resetting and discharging

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said diode, said switching circuit consisting of  
a first transistor for applying a reset  
pulse, and  
a second transistor for connecting said  
diode to a conductor within said multiconductor  
signal bus.

14. (Previously Presented) A solid state imaging  
device according to Claim 11, wherein said multiconductor  
signal bus comprises a plurality of vertically stacked  
conductors.

15. (Previously Presented) A solid state imaging  
device according to Claim 11, wherein said readout electronics  
are laterally adjacent one side of the image plane.

16. (Previously Presented) A solid state imaging  
device according to Claim 11, wherein said readout electronics  
are laterally adjacent two opposing sides of the image plane.

17. (Previously Presented) A solid state imaging  
device according to Claim 11, wherein all pixels of said array  
of pixels are reset simultaneously and are read out  
simultaneously.

Claim 18 (Claimed).

19. (Currently Amended) A solid state imaging device  
according to Claim 11, wherein each store circuit further

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comprises:

a third store circuitry ~~circuit~~ for storing a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

20. (Currently Amended) A solid state imaging device according to Claim 19, wherein said readout electronics further comprises:

a differential amplifier connected to said first, second and third store circuitry ~~circuits~~; and

a reset circuit for placing said differential amplifier in a common mode reset state prior to reading a signal.

21. (Currently Amended) A solid state imaging device comprising:

a two-dimensional array of pixels defining an image plane, the image plane comprising more than three rows of pixels, with each pixel comprising a photosensitive diode and a switching circuit for resetting and discharging said diode;

a multiconductor signal bus connected to said array of pixels, said multiconductor bus comprising a respective conductor to provide a dedicated readout channel for only one pixel of said two-dimensional array of pixels defining the image plane; and

readout electronics comprising a plurality of store circuits laterally adjacent the image plane and connected to said multiconductor signal bus for reading signals from said

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array of pixels, with a store circuit corresponding to each pixel and comprising

a first store circuitry ~~circuit~~ for storing a reset value, and  
a second store circuitry ~~circuit~~ for storing a read out value, with the read out value of a given pixel being modified by the stored reset value for that pixel.

22. (Previously Presented) A solid state imaging device according to Claim 21, wherein said switching circuit consists of:

a first transistor for applying a reset pulse; and  
a second transistor for connecting said diode to a conductor within said multiconductor signal bus.

23. (Previously Presented) A solid state imaging device according to Claim 21, wherein said signal bus comprises a multiconductor signal bus comprising a plurality of vertically stacked conductors.

24. (Previously Presented) A solid state imaging device according to Claim 21, wherein said readout electronics are laterally adjacent one side of the image plane.

25. (Previously Presented) A solid state imaging device according to Claim 21, wherein said readout electronics are laterally adjacent two opposing sides of the image plane.

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26. (Previously Presented) A solid state imaging device according to Claim 21, wherein all pixels of said array of pixels are reset simultaneously and are read out simultaneously.

Claim 27 (Cancelled).

28. (Currently Amended) A solid state imaging device according to Claim 21, wherein each store circuit further comprises:

a third store circuitry ~~circuit~~ for storing a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

29. (Currently Amended) A solid state imaging device according to Claim 28, wherein said readout electronics further comprises:

a differential amplifier connected to said first, second and third store circuitry ~~circuits~~; and

a reset circuit for placing said differential amplifier in a common mode reset state prior to reading a signal.

30. (Currently Amended) A method for making a solid state imaging device comprising:

defining an image plane using a two-dimensional array of pixels, the image plane comprising more than three rows of pixels;

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placing readout electronics comprising a plurality of store circuits laterally adjacent the image plane for reading signals from the array of pixels, with a store circuit corresponding to each pixel and comprising a first store circuitry ~~circuit~~ for storing a reset value, and a second store circuitry ~~circuit~~ for storing a read out value, with the read out value of a given pixel being modified by the stored reset value for that pixel; and

connecting a multiconductor signal bus connected between the array of pixels and the readout electronics, the multiconductor bus comprising a respective conductor to provide a dedicated readout channel for only one pixel of the two-dimensional array of pixels defining the image plane.

Claim 31 (Cancelled).

32. (Previously Presented) A method according to Claim 30, further comprising forming each pixel to have a photosensitive diode, and a switching circuit connected thereto for resetting and discharging the diode.

33. (Previously Presented) A method according to Claim 32, wherein the switching circuit consists of a first transistor for applying a reset pulse, and a second transistor for connecting the diode to a conductor within the multiconductor signal bus.

34. (Previously Presented) A method according to Claim 30, wherein the multiconductor signal bus comprises a

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plurality of vertically stacked conductors.

35. (Previously Presented) A method according to Claim 30, wherein the readout electronics are placed laterally adjacent one side of the image plane.

36. (Previously Presented) A method according to Claim 30, wherein the readout electronics are placed laterally adjacent two opposing sides of the image plane.

37. (Previously Presented) A method according to Claim 30, wherein the image device is configured so that all pixels of the array of pixels are reset simultaneously and are read out simultaneously.

Claim 38 (Cancelled).

39. (Currently Amended) A method according to Claim 30, wherein each store circuit further comprises a third store circuitry ~~circuit~~ for storing a second reset value, with a current reset value and a current read out value being processed simultaneously based upon application of a new reset pulse.

40. (Currently Amended) A method according to Claim 39, further comprising:

connecting a differential amplifier to the first, second and third store circuitry ~~circuits~~; and

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connecting a reset circuit to the differential  
amplifier for placing the differential amplifier in a common  
mode reset state prior to reading out a signal.